Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claims 1. - 20.(canceled)

Claim 21. (currently amended) An integrated circuit comprising:

a first transistor coupled between an input node and a first node;

a first ~~impendence~~ impedance matching circuit coupled between the first node and a second node;

a second ~~impendence~~ impedance matching circuit coupled between the second node and a third node;

a second transistor coupled between the third node and a fourth node;

a third ~~impendence~~ impedance matching circuit coupled between the fourth node and a fifth node; and

an ~~impendence~~ impedance transforming circuit coupled between the second node and the fifth node,

wherein in a first mode of operation, a signal provided at the input node passes through the first transistor, first ~~impendence~~ impedance matching circuit, and ~~impendence~~ impedance transforming circuit, and

in a second mode of operation, the signal provided at the input node passes through the first transistor, first ~~impendence~~ impedance matching circuit, second ~~impendence~~ impedance matching circuit, second transistor, and third ~~impendence~~ impedance matching circuit.

Claim 22. (currently amended) The integrated circuit of claim 21, wherein the ~~impendence~~ impedance transforming circuit comprises:

an inductance device coupled between the second node and a sixth node; and

a capacitor coupled between the sixth node and fifth node, wherein the inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

Claim 23. (currently amended) The integrated circuit of claim 21, wherein the ~~impendence~~ impedance transforming circuit comprises:

a capacitor coupled between the second node and a sixth node; and

an inductance device coupled between the sixth node and the fifth node, wherein the inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

Claim 24. (currently amended) The integrated circuit of claim 21, wherein the ~~impendence~~ impedance transforming circuit comprises:

a first capacitor coupled between the second node and a sixth node;

an inductance device coupled between the sixth node and the fifth node; and

a second capacitor coupled between the sixth node and a reference voltage level, wherein the inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

Claim 25. (currently amended) The integrated circuit of claim 21, wherein the ~~impendence~~ impedance transforming circuit comprises:

an inductance device coupled between the second node and a sixth node;

a first capacitor coupled between the sixth node and the fifth node; and

a second capacitor coupled between the sixth node and a reference voltage level, wherein the inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

Claim 26. (currently amended) The integrated circuit of claim 21, wherein the ~~impendence~~ impedance transforming circuit comprises:

an inductance device coupled between the second node and the fifth node; and

a capacitor coupled between the second node and the fifth node, wherein the inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

Claim 27. (currently amended) The integrated circuit of claim 21, wherein the ~~impendence~~ impedance transforming circuit comprises:

an inductance device coupled between the second node and the fifth node;

a first capacitor coupled between the second node and a reference voltage level; and

a second capacitor coupled between the fifth node and the reference voltage level. wherein the inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

Claim 28. (currently amended) The integrated circuit of claim 21, wherein the ~~impendence~~ impedance transforming circuit comprises:

an inductance device, coupled between the second node and the fifth node, wherein the inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

Claim 29. (currently amended) The integrated circuit of claim 21, wherein the third-~~impendence~~ impedance matching circuit comprises:

an inductance device coupled between the fourth node and the fifth node; and

a capacitor coupled between the fourth node and a reference voltage level, wherein the inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

Claim 30. (currently amended) The integrated circuit of claim 21, wherein the third ~~impendence~~ impedance matching circuit comprises:

a first capacitor coupled between the fourth node and a reference voltage level;

a first inductance device coupled between the fourth node and the reference voltage level; and

a second inductance device coupled between the fourth node and the fifth node, wherein the first inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide, and the second inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

Claim 31. (currently amended) The integrated circuit of claim 21, wherein the third ~~impendence~~ impedance matching circuit comprises:

a first inductance device coupled between the fourth node and a reference voltage level;

a first capacitor coupled between the fourth node and the reference voltage level;

a second inductance device coupled between the fourth node and the fifth node; and

a second capacitor coupled between the fifth node and the reference voltage level, wherein the first inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide, and the second inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

Claim 32. (currently amended) The integrated circuit of claim 21, wherein the third ~~impendence~~ impedance matching circuit comprises:

a first inductance device coupled between the fourth node and a reference voltage level;

a second inductance device coupled between the fourth node and the fifth node; and

a first capacitor coupled between the fifth node and the reference voltage level, wherein the first inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide, and the second inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

Claim 33. (currently amended) The integrated circuit of claim 21, wherein the third ~~impendence~~ impedance matching circuit comprises:

a first capacitor coupled between the fourth node and a reference voltage level;

a first inductance device coupled between the fourth node and the fifth node; and

a second inductance device coupled between the fifth node and the reference voltage level, wherein the first inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide, and the second inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

Claim 34. (currently amended) The integrated circuit of claim 21, wherein the first ~~impendence~~ impedance matching circuit comprises a first capacitor coupled between the first node and a second node, and wherein the second circuit comprises a second capacitor coupled between the second node and a third node.

Claim 35. (currently amended) The integrated circuit of claim 21, wherein the first ~~impendence~~ impedance matching circuit comprises no passive elements coupled between the first node and a second node, and the second ~~impendence~~ impedance matching circuit comprises a second capacitor coupled between the second node and a third node.

Claim 36. (currently amended) The integrated circuit of claim 34, wherein the first ~~impendence~~ impedance matching circuit further comprises an inductance device and a third capacitor, in series, coupled between the first node and a reference voltage level, wherein the inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

Claim 37. (previously presented) The integrated circuit of claim 36, wherein the inductance device is further coupled to a supply voltage level.

Claim 38. (previously presented) The integrated circuit of claim 34, wherein the second circuit further comprises an inductance device coupled between the second node and a reference voltage level, wherein the inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

Claim 39. (currently amended) The integrated circuit of claim 36, wherein the second ~~impendence~~ impedance matching circuit further comprises an inductance device coupled between the second node and the reference voltage level.

Claim 40. (currently amended) The integrated circuit of claim 34, wherein the second ~~impendence~~ impedance matching circuit further comprises an inductance device coupled between the third node and a reference voltage level, wherein the inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

Claim 41. (currently amended) The integrated circuit of claim 34, wherein the second ~~impendence~~ impedance matching circuit further comprises a third capacitor coupled between the second node and a reference voltage level.

Claim 42. (currently amended) The integrated circuit of claim 21, wherein the first ~~impendence~~ impedance matching circuit comprises an inductance device coupled between the first node and a reference voltage level, wherein the inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

Claim 43. (currently amended) The integrated circuit of claim 21, wherein the second ~~impendence~~ impedance matching circuit comprises:

a first capacitor coupled between the second node and a sixth node;

an inductance device coupled between the sixth node and a reference voltage level; and

a second capacitor coupled between the sixth node and the third node, wherein the inductance device comprises at least one of an inductor, wire bonding, transmission line, microstrip line, strip line, coaxial cable, or coplanar waveguide.

Claim 44. (previously presented) The integrated circuit of claim 21, further comprising

a voltage control circuit coupled to the second transistor, wherein the voltage control circuit, in response to a mode control voltage, provides a control signal to the second transistor to place the second transistor in an on state or an off state.

Claim 45. (previously presented) The integrated circuit of claim 44, wherein the voltage control circuit comprises a third transistor coupled between the second transistor and a reference voltage level, wherein an electrode of the third transistor is coupled to a voltage control line.

Claim 46. (previously presented) The integrated circuit of claim 44, wherein the voltage control circuit comprises a third transistor coupled between the second transistor and a reference voltage level and a fourth transistor coupled between a supply voltage line and a reference voltage level, wherein an electrode of the third transistor is connected to the coupled point of the fourth transistor toward the supply voltage line and an electrode of the fourth transistor is coupled to a voltage control line.

Claim 47. (previously presented) The integrated circuit of claim 44, wherein the voltage control circuit comprises a third transistor coupled between the second transistor and a reference voltage level and a fourth transistor coupled between a supply voltage line and an electrode of the third transistor, wherein an electrode of the third transistor is coupled to the fourth transistor and an electrode of the fourth transistor is coupled to a voltage control line.

Claims 48.- 52. (canceled)

Claim 53. (previously presented) The integrated circuit of claim 21, wherein the first transistor or the second transistor is a bipolar junction transistor, a heterojunction bipolar transistor, a field effect transistor, a complementary metal-oxide semiconductor transistor, a metal-oxide semiconductor transistor, p-type metal-oxide semiconductor transistor, n-type meta - oxide semiconductor transistor, a high electron mobility transistor, or a metal semiconductor field effect transistor.

Claims 54. - 127 (canceled)

Claim 128. (previously presented) An amplifier circuit comprising:

an input node configured to couple a signal transmitted through a first set of impedance matching networks coupled in series between the input node and a second node;

a second set of impedance matching network and a power amplification stage coupled in series between the second node and a third node, wherein at least one of the second set of impedance matching networks provides a low impedance signal path to the signal in a firs operational state of the amplifier circuit and a high impedance path to the signal in a second operational state of the amplifier circuit; and

a set of impedance transforming networks coupled in parallel to the second set of impedance matching networks and the power amplification stage, wherein the set of impedance transforming networks in cooperation with the first set of impedance matching networks provides a low impedance path to the signal when the second set of impedance matching networks in cooperation with the first set of impedance matching networks and power amplification stage provides a high impedance path to the signal.

Claim 129. (previously presented) The amplifier circuit of claim 128, wherein the first set of impedance matching networks comprises at least one impedance matching network.

Claim 130. (previously presented) The amplifier circuit of claim 128, wherein the second set of impedance matching networks comprises at least one impedance matching network.

Claim 131. (previously presented) The amplifier circuit of claim 128, wherein the power amplification stage is responsive to a voltage control signal, wherein when the voltage control signal is at a first level, the power amplification stage is set to attenuate the signal, and when the voltage control signal is at a second level, the power amplification stage is set to amplify the signal.

Claim 132. (currently amended) The amplifier circuit of claim 128, wherein when in the first operational state, the signal path defined by the first set of impedance matching networks, the second set of impedance matching networks, and the power amplification stage provides a low ~~impendence~~ impedance path for the signal between the input node and the third node.

Claim 133. (currently amended) The amplifier circuit of claim 128, wherein when in the first operational state, the signal path defined by the first set of impedance matching networks and the set of impedance transforming networks provides a high ~~impendence~~ impedance path for the signal between the input node and the third node.

Claim 134. (previously presented) The amplifier circuit of claim 128, wherein when in the second operational state, the signal path defined by the first set of impedance matching networks, the second set of impedance matching networks, and the power amplification stage provides a high ~~impendence~~ impedance path for the signal between the input node and the third node.

Claim 135. (currently amended) The amplifier circuit of claim 128, wherein when in the second operational state, the signal path defined by the first set of impedance matching networks and the set of impedance transforming networks provides a low ~~impendence~~ impedance path for the signal between the input node and the third node.

Claim 136. (currently amended) A method of amplifying a signal, the method comprising:

transmitting a signal along a first signal path defined by a first set of ~~impendence~~ impedance matching networks and a power amplification stage, wherein the first signal path is disposed between an input node and an output node;

transmitting the signal along a second signal path defined by the first set of ~~impendence~~ impedance matching networks and a set of impedance transforming networks coupled in series between the input node and the output node, wherein the set of impedance transforming networks define a segment of the second signal path disposed in parallel with the first signal path; and

configuring the first signal path and the second signal path to different impedance states with respect to a mode of signal amplification.

Claim 137. (previously presented) The method of claim 136, further comprising configuring the first signal path to a low impedance state and the second signal path to high impedance state when in a first power mode.

Claim 138. (previously presented) The method of claim 137, further comprising configuring the power amplification stage to amplify the signal when in the first power mode state.

Claim 139. (previously presented) The method of claim 137, further comprising configuring the power amplification stage to attenuate the signal when in a second power mode.

Claim 140. (currently amended) The method of claim 136, further comprising transmitting the signal from the input node to an input of the second set of ~~impendence~~ impedance matching networks and an input of the set of impedance transforming networks.

Claim 141. (previously presented) The method of claim 140, wherein when in a first power mode a majority of the signal is transmitted along the second signal path and reflected from the first signal path.

Claim 142. (previously presented) The method of claim 140, wherein when in the second power mode a majority of the signal is transmitted along the first signal path and reflected from the second signal path.